Global CNOT Synthesis with Holes

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Limitations of NISQ Computers

Connectivity Constraints



Constraint Topology



Limitations of NISQ Computers

Connectivity Constraints



Constraint Topology



- Compilation method to overcome NISQ computers shortcommings
- Usually works for circuits made from a specific gate set
- Generates improved circuit, e.g with fewer gates or respecting connectivity constraints, from an efficent representation of the original circuit

Unitary Decomposition Gate Sets



Unitary Decomposition Slicing



Unitary Decomposition Slicing



Unitary Decomposition

Quantum Combs



The problem now becomes how to synthesise a quantum comb

CNOT Synthesis







CNOT Combs



Circuit Representation

Identity Gate $|x\rangle \longrightarrow |x\rangle$ $|y\rangle \longrightarrow |y\rangle$ CNOT Gate $|x\rangle \longrightarrow |x\rangle$ $|y\rangle \longrightarrow |x \oplus y\rangle$

CNOT(c, t) corresponds to R(c, t)

Identity Parity Matrix $x \quad y$ $x' \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$ CNOT Parity Matrix $x \quad y$ $x' \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$ CNOT Parity Matrix

Circuit Representation



CNOT(c, t) corresponds to R(c, t)

RowCol - Synthesis Algorithm for CNOT Circuits $_{\mbox{\sc Algorithm}}$

- RowCol reduces a parity matrix to the identity by eliminating the row and column for each qubit.
- RowCol can synthesise to constrained architecures:
 - Qubit being eliminated has to correspond to non-cutting vertex.
 - This is done using Steiner trees.

Eliminate Row 1 and Column 1:

$$\begin{pmatrix} 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{pmatrix} \xrightarrow{R_1 := R_0 + R_1} \begin{pmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{pmatrix} \xrightarrow{R_0 := R_3 + R_0} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{pmatrix}$$

Eliminate Column 2:

$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{pmatrix} \xrightarrow{R_1 := R_2 + R_1} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{pmatrix} \xrightarrow{R_1 := R_3 + R_1} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{pmatrix}$$

Eliminate Column 3:

$$\left(\begin{array}{rrrrr} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{array}\right) \xrightarrow{R_2 := R_3 + R_2} \left(\begin{array}{rrrrr} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{array}\right)$$

We have reached the identity matrix meaning our synthesis process is over.





Old Circuit





$$\mathcal{H} = \{(1,4), (2,6), (6,7), (4,5)\}$$

$$t(0) = 0, t(1) = 5, t(2) = 7, t(3) = 3$$



A temporal qubit can be extracted if its row and column in the full parity matrix can be eliminated by only row operations on the submatrix.

		Init	ial	sub	-ma	atri	x			EI	imi	nate	ed s	sub-	ma	trix	[Row operations required for reduction
	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		
0	0 /	0	0	1	1	0	1	1	0	0 /	0	0	1	1	0	1	1		
5	0	0	0	0	0	1	0	0	5	0	0	0	0	0	1	0	0		
7	1	1	0	1	1	0	1	1	7	1	1	0	1	1	0	1	1		N/A
3	$\setminus 1$	1	0	1	0	0	0	0/	3	$\setminus 1$	1	0	1	0	0	0	0)	

$$\mathcal{H} = \{(1,4), (2,6), (6,7), (4,5)\}$$

$$t(0) = 0, t(1) = 5, t(2) = 7, t(3) = 3$$



 $\mathcal{H} = \{(1,4), (2,6), (6,7)\}$

$$t(0) = 0, t(1) = 4, t(2) = 7, t(3) = 3$$

		انما	ial	cub		.++;						nati				+ - :	,		Row operations
		Init	lai	suc)-m	atri	х				Imii	nate	ea s	sub-	·ma	trix			required for reduction
	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		
0	/ 1	1	0	0	0	0	0	0 \	0	(1)	1	0	0	0	0	0	0		
4	1	1	0	0	1	0	1	0	4	0	0	0	1	1	0	0	0		D(c, A) = D(2, c)
6	1	1	0	1	0	0	1	0	6	0	0	0	0	0	0	1	0		R(0, 4), R(3, 0)
3	$\overline{1}$	1	0	1	0	0	0	0/	3	1	1	0	1	0	0	0	0)	

 $\mathcal{H} = \{(1, 4), (2, 6)\}$

$$t(0) = 0, t(1) = 4, t(2) = 6, t(3) = 3$$

		الما	ial	cub		.++;						+	. d. c			+			Row operations
		IIIII	Idi	sub	-111	atri	X					ale	eu s	sub-	ma	LLIX			required for reduction
	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		
0	/ 1	1	0	0	0	0	0	0 \	0	(1)	1	0	0	0	0	0	0		
4	0	0	0	1	1	0	0	0	4	1	1	0	0	1	0	0	0		D(2, A) = D(0, 2)
2	1	0	1	0	0	0	0	0	2	1	0	1	0	0	0	0	0		R(3, 4), R(0, 3)
3	1	1	0	1	0	0	0	0 /	3	0	0	0	1	0	0	0	0)	

 $\mathcal{H} = \{(1,4)\}$

$$t(0) = 0, t(1) = 2, t(2) = 7, t(3) = 3$$

		Init	ial	cub	m	tri	~				FI	mi	hot.	ad a	ub	ma	+riv			Row operations
		min	.141	Sub	-1116	aun	^						ald	su s	sub-	IIIa				required for reduction
	0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7		
0	(1)	1	0	0	0	0	0	0 \	\setminus	0	(1)	1	0	0	0	0	0	0 `)	
4	1	1	0	0	1	0	0	0		4	0	0	0	0	1	0	0	0		P(0, A)
2	1	0	1	0	0	0	0	0		2	1	0	1	0	0	0	0	0		(0, 4)
3	0	0	0	1	0	0	0	0	/	3	0	0	0	1	0	0	0	0)	

 $\mathcal{H} = \{(1,4)\}$

$$t(0) = 0, t(1) = 4, t(2) = 2, t(3) = 3$$

		ا سا		h		- + :	.,			EI:		t .				.			Row operations
		Init	lai	suc)-m	atri	x				mII	late	ea s	sub-	·ma	τηχ			required for reduction
	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		
0	1	1	0	0	0	0	0	0	0 /	1	0	0	0	0	0	0	0)	
1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0		P(0, 2) P(1, 0)
2	1	0	1	0	0	0	0	0	2	0	1	1	0	0	0	0	0		R(0, 2), R(1, 0)
3	0	0	0	1	0	0	0	0/	3 \	0	0	0	1	0	0	0	0)	

$$\mathcal{H} = \{\}$$

$$t(0) = 0, t(1) = 1, t(2) = 2, t(3) = 3$$

Initial sub-matrix									EI	imiı	nate	ed s	sub-	ma	trix			Row operations	
	0	1	2	2	1	E	6	7		0	1	2	2	Λ	E	6	7		required for reduction
	0	Т	2	С	4	5	0	1		0	Т	Ζ	З	4	5	0	1		
0	(1)	0	0	0	0	0	0	0 \	0	(1)	0	0	0	0	0	0	0 `		
1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0		P(1,2)
2	0	1	1	0	0	0	0	0	2	0	0	1	0	0	0	0	0		R(1,2)
3	0	0	0	1	0	0	0	0/	3	0 /	0	0	1	0	0	0	0	/	

$$\mathcal{H} = \{\}$$

$$t(0) = 0, t(1) = 1, t(2) = 2, t(3) = 3$$

Row Operations: R(7,0), R(3,7), R(4,7), R(0,7), R(6,4), R(3,6), R(3,4), R(0,3), R(0,4), R(0,2), R(1,0), R(1,2)

Holes: $\mathcal{H} = \{(1, 4), (2, 6), (6, 7), (4, 5)\}$

Plugs: $p :: \{(1,4) \mapsto V, (4,5) \mapsto H, (2,6) \mapsto U, (6,7) \mapsto W\}$



Slicing



Experimental Parameters

Architectures

- 9q-square
- 16-square
- regetti_16q_aspen
- ∎ bm_qx5
- ibm_q20_tokyo

CNOT Count

481632

1024

Non-CNOT Proportion

5%

15%

25%

50%

Graph Selection



	59	%
Architectures	Non-CNC	OT Gates
	Comb	Slice
9q-square	-43.1%	80.79%
16q-square	13.11%	344.5%
regetti₋	17 31%	555 1%
16q_aspen	47.31/0	555.470
bm_qx5	32.27%	461.9%
ibm_q20_tokyo	33.17%	393.1%

	15	5%
Architectures	Non-CNC	OT Gates
	Comb	Slice
9q-square	34.12%	208.7%
16q-square	154.4%	511.1%
regetti₋	231.2%	803 1%
16q_aspen	231.270	095.170
bm_qx5	197.2%	698.8%
ibm_q20_tokyo	183.6%	481.0%

	25	5%
Architectures	Non-CNC	OT Gates
	Comb	Slice
9q-square	91.93%	255.9%
16q-square	263.9%	564.6%
regetti₋	370.6%	1027%
16q_aspen	579.070	1027/0
bm_qx5	322.4%	783.6%
ibm_q20_tokyo	289.3%	500.2%

	50	1%
Architectures	Non-CNC	OT Gates
	Comb	Slice
9q-square	182.1%	306.8%
16q-square	437.0%	606.9%
regetti₋	614 0%	1110%
16q_aspen	014.970	111970
bm_qx5	527.8%	837.7%
ibm_q20_tokyo	440.7%	498.2%

- Proposed using quantum combs as an alternative to slicing for generalising circuit synthesis
- Introduced CombSynth, a synthesis algorithm for CNOT combs based on RowCol
- Tested CombSynth against RowCol with slicing and found it performed better on a wide variety of experimental parameters.

Future Work

Other Gate Sets



Future Work

Compare with literature

Investigate how synthesis with quantum combs relates to compilation methods that don't use slicing:

- ZX Circuit Extraction : Duncan, Kissinger, Perdrix and van de Wetering 2019
- Lazy Synthesis : Martiel and Goubault de Brugière 2020